Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer over and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

forming a liner upon a sidewall of each said isolation trench;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer, and said depositing is

carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench and extending over said spacers and over said first dielectric layer; and

planarizing the conformal layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

2. (Cancelled).

3. (Previously presented) A method according to Claim 1, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

4. (Previously presented) A method according to Claim 1, wherein forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter.

5. (Original) A method according to Claim 1, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

6. (Original) A method according to Claim 1, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

7. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has an edge;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal layer and said depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing with a single etch recipe the conformal layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein:

said planarizing is performed in the absence of masking the conformal layer over each said isolation trench;

material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

said conformal layer and said spacers form said upper surface for each said isolation trench, each said upper surface being formed from said conformal layer and said spacer and being situated above said pad oxide layer; and

said first dielectric layer is in contact with at least a pair of said spacers and said pad oxide layer.

8. (Original) A method according to Claim 7, further comprising:

removing said pad oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

9. (Previously presented) A method according to Claim 7, wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

10. (Original) A method according to Claim 9, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

11. (Original) A method according to Claim 7, wherein said upper surface for each said isolation trench is formed by the steps comprising:

chemical mechanical planarization, wherein said conformal layer, said spacers, and said first dielectric layer form a planar first upper surface; and

an etch that forms a second upper surface, said second upper surface being situated above said pad oxide layer.

12. (Original) A method according to Claim 11, wherein said etch uses an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

13. (Currently Amended) A method according to Claim 12 ~~Claim 11~~, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

14. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon said oxide layer;

selectively removing said silicon nitride layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

forming a corresponding electrically active region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, said liner being confined preferentially within each said isolation trench and extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal second silicon dioxide layer, said conformal second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second silicon dioxide layer, and said depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench and extending over said spacers and said silicon nitride layer; and

selectively removing said conformal second silicon dioxide layer and said spacers to form an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and being situated above said pad oxide layer, wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches, and wherein said selectively removing is performed in the absence of masking the conformal second silicon dioxide layer over each said isolation trench.

15. (Original) A method according to Claim 14, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

16. (Original) A method according to Claim 14, wherein said liner is composed of silicon nitride.

17. (Original) A method according to Claim 15, further comprising:

removing said oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

18. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said

spacers, wherein said filling is performed by depositing said conformal third layer, and said depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein planarizing the conformal third layer to form therefrom said upper surface for each said isolation trench that is co-planar to the other said upper surfaces further comprises planarizing said conformal third layer and each said spacer to form therefrom said co-planar upper surfaces, and said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

19. (Original) A method according to Claim 18, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

20. (Original) A method according to Claim 18, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

21. (Currently Amended) A method according to Claim 18 , further comprising, prior to filling each said isolation trench with said conformal third layer, forming a liner upon a sidewall of each said isolation trench, said liner being confined preferentially within each said isolation trench and extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate, and wherein said conformal third layer is composed of an electrically insulative ~~conductive~~ material.

22. (Original) A method according to Claim 21, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

23. (Original) A method according to Claim 21, wherein forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter.

24. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said

spacers, wherein said filling is performed by depositing said conformal third layer, and said depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein said upper surface for each said isolation trench is formed from said conformal third layer, said spacers, and said first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

25. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said

spacers, wherein said filling is performed by depositing said conformal third layer, and said depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate;

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers; and

selectively removing said third layer, said spacers and said layer composed of polysilicon to form a portion of at least one of said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

26. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer, wherein said forming a second dielectric layer includes forming a second dielectric layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

rounding the top edges of each of said isolation trenches;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said

spacers, wherein said filling is performed by depositing said conformal third layer, and said depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench and extending over said spacers and over said first dielectric layer;

planarizing the conformal third layer by an etch using an etch recipe that etches said first dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from of about 1:1 to about 2:1 to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing the conformal third layer is performed in the absence of masking the conformal third layer over each of said isolation trenches;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches.

27. (Original) A method according to Claim 26, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

28-30. (Cancelled)

31. (Currently Amended) A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a silicon nitride layer upon said polysilicon layer;

selectively removing said silicon nitride layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer, wherein said forming a first silicon dioxide layer includes forming a first silicon dioxide layer on and in contact with the exposed oxide layer at said plurality of areas;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is in contact with said silicon nitride layer and said polysilicon layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer and from top edges into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding doped region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, each said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

rounding the top edges of said isolation trenches;

filling each said isolation trench with a conformal second layer, said second layer extending above said oxide layer in contact with a corresponding pair of said spacers, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench and extending over said spacers and over said silicon nitride layer; and

planarizing said conformal second layer and each of said spacers to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and is situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

32. (Previously presented) A method according to Claim 31, wherein each said liner is a thermally grown oxide of said semiconductor substrate, and wherein said conformal second layer is composed of an electrically insulative material.

33. (Previously presented) A method according to Claim 31, wherein each said liner is composed of silicon nitride, and wherein said conformal second layer is composed of an electrically insulative material.

34. (Previously presented) A method according to Claim 31, further comprising:

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate; and

forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and

selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces.

35. (Currently Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

selectively removing said first layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the exposed oxide layer at said plurality of areas, wherein electrically insulative material extends continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of filling ~~leaving no gap within~~ each said isolation trench and extending over said spacer and over said first layer;

having a top edge and said top edge being rounded; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer, wherein said planar upper surface is formed by planarizing in the absence of masking said second layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

36. (Original) The method as defined in Claim 35, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each said isolation trench.

37. (Original) The method as defined in Claim 36, wherein the doped trench bottom has a width, each said the isolation trench has a width, and the width of each said doped trench bottom is greater than the width of the respective isolation trench.

38. (Currently Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

selectively removing said first layer to expose said oxide layer at a plurality of areas;

forming a plurality of isolation trenches through the oxide layer at said plurality of areas, wherein electrically insulative material extends continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer, wherein said filling is performed by depositing said second layer, and said depositing is carried out to the extent of filling ~~leaving no gap within~~ each said isolation trench and extending over said spacer and over said first layer;

having a top edge and said top edge being rounded; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer, wherein said planar upper surface is

formed by planarizing in the absence of masking said second layer over each of said isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

39. (Original) The method as defined in Claim 38, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of said isolation trenches.

40. (Original) The method as defined in Claim 39, wherein:

the doped trench bottom has a width;

each said isolation trench has a width; and

the width of each said doped trench bottom is greater than the width of the respective isolation trench.

41. (Cancelled)

42. (Currently Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at top edges at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is curved;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

rounding the top edges of said isolation trenches;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of filling ~~leaving no gap within~~ each of said isolation trenches and extending over said spacers and over said first layer; and

forming with a single etch recipe a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

43. (Currently Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said

second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, conformally filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures, wherein said filling is performed by depositing said conformal second layer, and said depositing is carried out to the extent of filling ~~leaving no gap within~~ each of said isolation trenches and extending over said spacers and over said first layer; and

planarizing the conformal second layer and said first and second spacers of said respective first and second isolation structures to form a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation

trenches, and wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches.

REMARKS

By this amendment, claims 1, 7, 13, 14, 18, 24-26, 31, 35, 38, 42, and 43 have been amended and claim 2 has been cancelled. Accordingly, claims 1, 3-27, 31-40, 42, and 43 are pending in the present application. The claim amendments are supported by the specification, the accompanying figures, and claims as originally filed, with no new matter being added. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

1. Objections to the Drawings

The drawings have been objected for failing to show "forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter" in claim 4 and "removing said pad oxide" and "forming a gate oxide layer" in claim 8. Applicants respectfully traverse.

First, "forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter" is described at page 12, ll. 14-17, "Another method of forming insulation liner 30 is CVD of a dielectric material, or a dielectric material precursor that deposits preferentially upon sidewall 50 of isolation trench 32." Hence liner 30 in Figures 5A and 5B illustrate the cited deposition of a composition of matter.

Next, "removing said pad oxide" and "forming a gate oxide layer" are shown in Figures 7-8 whereby the pad oxide 14 is removed and the gate oxide layer 44 is added. *See* page 16, ll. 9-14.

Accordingly, the prompt removal of these objections is respectfully requested.

2. Objection Under 37 C.F.R. § 1.75(c)

Claims 2 and 34 have been objected to under 37 C.F.R. § 1.75(c) for being of improper dependent form for failing to further limit the subject matter of a previous claim. In particular, the Office Action states that claim 2 recites a limitation that is recited in present claim 1. In addition, the Office Action states that claim 34 recites "a layer composed of polysilicon upon said gate oxide" when it should recite "a layer composed of polysilicon upon said oxide layer."

Claim 2 has been cancelled. Regarding claim 34, however, Applicants respectfully direct the Examiner to Figure 8B, wherein a polysilicon layer 24 is formed over a gate oxide layer 44. The polysilicon layer 24 is formed over the gate oxide layer 44 after the pad oxide layer was removed. *See e.g.* Specification at p. 16, ll. 9-14 and p. 19, ll. 10-16.

Applicants therefore respectfully request the prompt removal of this objection.

3. Objections Under 37 U.S.C.. § 132

The amendment filed February 12, 2002 has been objected to because it introduces new matter. Applicants respectfully traverse.

First, the claims have been objected to for including the recitation, "depositing is carried out to the extent of leaving no gap in each said isolation trench." In response, each instance of the limitation has been amended to recite some form of "depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench." Support for this limitation can be found in the application as filed at page 13, lines 22-24.

Next, the claims have also been objected to for including the recitation, "wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench."

See e.g. claim 1. Operations such as planarizing and selective removing are performed by chemical mechanical planarization or polishing (CMP) in embodiments of this invention that are disclosed in the Application. See, e.g., Application, p. 3, ll. 25-26, p. 6, ll. 1-3, p. 15, l. 4, p. 20, ll. 15-17. The practice of CMP does not rely on masking, but it is known in contrast for its use to achieve an overall planar surface, sometimes referred to as global planarity. A rotating table typically holds the wafer in this CMP process and an appropriate slurry is supplied between the wafer and a polishing pad that is applied to the wafer at a specified pressure. Applicants submit that this knowledge of a person of ordinary skill in the art together with the disclosure in the Application of CMP for selective removing and/or planarizing show possession of the claimed invention.

Finally, the claims have also been objected to for including the recitation, "liner being confined within each isolation trench." The relevant limitations in the claims have been amended to recited, "liner being confined preferentially within each isolation trench." Support for this limitation can be found, *e.g.*, in the application as filed at page 12, line 14-16, which states "CVD of a dielectric material, or a dielectric precursor material that deposits *preferentially* upon sidewall 50 of isolation trench 32. Thus, at least one exemplary method, the particulars of which are well known in the art is referenced in the specification for forming a liner within a trench. Such a method would be understood as including steps not expressly recited in the specification. Accordingly, the prompt removal of this rejection is respectfully requested.

Accordingly, Applicants respectfully request the prompt removal of the objection under 37 U.S.C. § 132.

4. Rejections Under 35 U.S.C. §§ 112(1)

Claims 1-27, 31-40, 42, and 43 have been rejected under 35 U.S.C. § 112, first paragraph, for containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time of the application was filed, had possession of the claimed invention. Applicants respectfully traverse.

Initially, the claims have been rejected for including the recitation, "depositing is carried out to the extent of leaving no gap in each said isolation trench." In response, each instance of the limitation has been amended to recite some form of "depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench." Support for this limitation can be found in the application as filed at page 13, lines 22-24.

Next, the claims have also been rejected for including some form of the limitation: "wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench." *See e.g.* claim 1. Operations such as planarizing and selective removing are performed by chemical mechanical planarization or polishing (CMP) in embodiments of this invention that are disclosed in the Application. See, e.g., Application, p. 3, ll. 25-26, p. 6, ll. 1-3, p. 15, l. 4, p. 20, ll. 15-17. The practice of CMP does not rely on masking, but it is known in contrast for its use to achieve an overall planar surface, sometimes referred to as global planarity. A rotating table typically holds the wafer in this CMP process and an appropriate slurry is supplied between the wafer and a polishing pad that is applied to the wafer at a specified pressure. Applicants submit that this knowledge of a person of ordinary skill in the art together with the disclosure in the Application of CMP for selective removing and/or planarizing show possession of the claimed invention.

Accordingly, the prompt removal of the foregoing rejection of claims 1-27, 31-40, 42, and 43

under 35 U.S.C. § 112, first paragraph, is respectfully requested.

Claims 4, 16, and 21 have been rejected for reciting under 35 U.S.C. § 112, first paragraph, "because the specification . . . does not reasonable provide enablement for rounding the top edge of trench by depositing material on the trench surface." Applicants respectfully traverse.

In response, Applicants note that claims 4 and 21 recite the formation of a liner and the step of rounding the top edge of the trench as separate limitations. Further, neither the claims nor the specification require that the step of rounding the top edge of the trench be performed by depositing material. Accordingly, enablement of "rounding the top edge of trench by depositing material on the trench surface" is not necessary and the prompt removal of this rejection is respectfully requested. The rejection of claim 16 appears to be in error.

Claims 14-17 and 21-23 have been rejected for reciting under 35 U.S.C. § 112, first paragraph, "because the specification . . . does not reasonable provide enablement for depositing CVD, the liner 30 to be confined within each isolation trench." Applicants respectfully traverse.

Present claim 14 now recites, "said liner being confined preferentially within each said isolation trench." Support for this limitation can be found, *e.g.*, in the application as filed at page 12, line 14-16, which states "CVD of a dielectric material, or a dielectric precursor material that deposits preferentially upon sidewall 50 of isolation trench 32. Thus, at least one exemplary method, the particulars of which are well known in the art is referenced in the specification for forming a liner within a trench. Such a method would be understood as including steps not expressly recited in the specification. Accordingly, the prompt removal of this rejection is respectfully requested.

Applicants therefore respectfully request the prompt withdrawal of the foregoing rejections of the claims under 35 U.S.C. § 112, first paragraph.

5. Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1-26 and 31-40 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner has inquired as to the meaning of, "wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches." Applicants respectfully traverse.

Regarding what the limitation, "wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches" refers to, Applicants direct the Examiner to Figure 9 of the application as filed, wherein a plurality of isolation trenches are depicted having continuous material(s) extending into and connecting each isolation trench. As further depicted in Figure 5-8, it can be seen that this continuous material(s) is derived from the electrically insulative materials oxide layer 14, spacer 28, and isolation film 36. *See e.g.* p. 9, ll. 7-10. In various places in the application each of the oxide layer, the spacers, and the isolation film are identified as electrically insulative materials, although not verbatim with that language. Accordingly, the prompt removal of this rejection is respectfully requested.

Claim 13 has been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner has indicated that "wherein said ratio in a range from about 1.3"1 to about 1.7:1 lacks support in the parent claims 7 and 13. Applicants respectfully traverse.

Claim 13 has been amended to claim dependency from claim 12, which recites a ratio and thereby provides antecedent basis. The prompt removal of this rejection is therefore respectfully requested.

Claims 9, 10, 12, 13, 26, 27, 29, and 30 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the office action states that the limitation of claim 9 "wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1," and the like, lack antecedent basis. Applicants respectfully traverse.

Initially, Applicants respectfully note that claims 29 and 30 have been cancelled and so this rejection is inapplicable to them. Regarding the use of the term "selective to" in the specification, Applicant directs the Examiner to page 15, lines 11-15. That passage states in part, "Reduced island 52 is preferably removed with an etch that is selective to isolation film 36 and spacer 28, leaving an isolation structure 48 that extends into and above isolation trench 32, forming a nail shaped structure having a head 54 extending above and away from isolation trench 32 upon an oxide layer 44." It is therefore clear that, as used in the specification, the term "selective to" indicates that a material is etched more slowly than other materials. Hence, a correct reading of page 14, lines 14-25 of the specification is consistent with the specification by indicating that "planarization will be selective to isolation film 26." Accordingly, the prompt removal of this rejection is respectfully requested.

Claims 21-23 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention and as failing to correspond in scope to what Applicants regard as the invention. In particular, the Examiner states that the phrase "electrically conductive material" lacks antecedent basis. In addition, the Examiner notes in section 12 of the Office Action that claims 21-

23 fail to correspond in scope with that which the Applicants regard as the invention. Applicants respectfully traverse.

Claim 21 has been amended to recite: "wherein said conformal third layer is composed of an electrically insulative [conductive] material." Accordingly, the prompt removal of this rejection is respectfully requested.

Claims 1-27, 31-40, 42, and 43 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More particularly, the Office Action states that claims 1-27, 31-40, 42, and 43 state what the inventors did not invent rather than what they did invent through the limitations, "depositing is carried out to the extent of leaving no gap in each said isolation trench" and "planarizing is performed in the absence of masking the conformal layer over each said isolation trench." Applicants respectfully traverse.

Initially, each instance of the limitation "depositing is carried out to the extent of leaving no gap in each said isolation trench" has been amended to recite some form of "depositing is carried out to the extent of filling ~~leaving no gap in~~ each said isolation trench." Support for this limitation can be found in the application as filed at page 13, lines 22-24.

Regarding the limitation, "planarizing is performed in the absence of masking the conformal layer over each said isolation trench," Applicants respectfully disagree with the rejection. The section of the MPEP cited by the Examiner states in part:

> The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection sought are set forth definitely, albeit negatively, the claim complies with the requirements of 35 U.S.C. 112, second paragraph.

* * *

The mere absence of a positive recitation is not basis for an exclusion.

MPEP 2173.05(i), 8th ed. Rev. 1, (emphasis added). Operations such as planarizing and selective removing are performed by chemical mechanical planarization or polishing (CMP) in embodiments of this invention that are disclosed in the Application. See, e.g., Application, p. 3, ll. 25-26, p. 6, ll. 1-3, p. 15, l. 4, p. 20, ll. 15-17. The practice of CMP does not rely on masking, but it is known in contrast for its use to achieve an overall planar surface, sometimes referred to as global planarity. A rotating table typically holds the wafer in this CMP process and an appropriate slurry is supplied between the wafer and a polishing pad that is applied to the wafer at a specified pressure. Applicants submit that this knowledge of a person of ordinary skill in the art together with the disclosure in the Application of CMP for selective removing and/or planarizing clearly delineate the bounds of the claimed invention. Accordingly, the prompt removal of this rejection is respectfully requested.

6. Rejections Under 35 U.S.C. 103(a)

Claims 1-4, 6-13, 18, 19, and 21-27 have been rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,097,072 to Omid-Zohoor, et al., ("the '072 patent") in view of U.S. Patent No. 6,184,108 to Omid-Zohoor et al., ("the '108 patent"). Applicants respectfully traverse.

Present independent claims 1, 7, 18, and 24-26, recite, among other things and with language variations in each claim, "planarizing the *conformal layer* ... to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (emphasis added).

In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse-resist mask 368 over trench regions 356 (*see* the '072 patent, Fig. 3K, col. 4, *ll.* 51-52) to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a remaining oxide layer 364 with ridges 373 (*see* the '072 patent, Fig. 3L, col. 4, *ll.* 52-54). It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing until silicon nitride layer 344 is exposed (*see* the '072 patent, Fig. 3M, col. 4, *ll.* 54-57, 59-61). Accordingly, the method disclosed in the '072 patent does not *planarize the conformal oxide layer* 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps.

Additionally, present claim 7 recites the use of a single etch recipe to form a planar upper surface from the conformal layer. In contrast, the method disclosed in the '072 patent, as previously noted, uses a multi-step method with different etch recipes to form a planar upper surface.

Further, claims 1, 7, 18, and 24-26 recite some form of planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, the '072 patent discloses a more

complicated method that involves masking of a conformal layer and other steps.

Claims 2-4, 6, 8-13, 19, 21-23, and 27 depend from one of independent claims 1, 7, 18, and 24-26, respectively, and include the limitations recited therein. Accordingly, for at least the reasons presented above with respect to claims 1, 7, 18, and 24-26, claims 2-4, 6, 8-13, 19, 21-23, and 27 are not obviated by the '072 patent and the '108 patent. Accordingly, the prompt removal of the rejection of claims 1-4, 6-13, 18, 19, and 21-27 is respectfully requested.

Claims 14-17 and 31-34 have been rejected under 35 U.S.C. § 103(a) over the '072 patent in view of U. S. Patent No. 5,387,540 to Poon et al ("*Poon*") for the reasons stated on pages 21-26 of the Office Action. Applicants respectfully traverse.

Present claim 31 recites, among other things and with language variations in each claim, "planarizing the *conformal layer* ... to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (emphasis added).

In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse-resist mask 368 over trench regions 356 (*see* the '072 patent, Fig. 3K, col. 4, *ll.* 51-52) to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a remaining oxide layer 364 with ridges 373 (*see* the '072 patent, Fig. 3L, col. 4, *ll.* 52-54). It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing until silicon nitride layer 344 is exposed (*see* the '072 patent, Fig. 3M, col. 4, *ll.* 54-57, 59-61). Accordingly, the method disclosed in the '072 patent does not *planarize the conformal oxide layer* 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps.

Further, claims 14 and 31 recite some form of planarization that is performed in the absence

of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, the '072 patent discloses a more complicated method that involves masking of a conformal layer and other steps.

Regarding claim 34, the '072 patent does not teach or suggest forming between said isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces. Consequently, the '072 patent does not teach or suggest the presently claimed methods with the features recited in claim 34.

Further, claims 1, 7, 14, 18, 24-26, 31, 35, 38, and 42 recite some form of planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, the '072 patent discloses a more complicated method that involves masking of a conformal layer and other steps.

Poon cannot cure the foregoing deficiencies of the '072 Patent. Claims 15-17 and 32-34 depend from one of independent 14 and 31, respectively, and include the limitations recited therein. Accordingly, for at least the reasons presented above with respect to claims 14 and 31, claims 15-17 and 32-34 are not obviated by the '072 patent in view of *Poon*. Accordingly, the prompt removal of the rejection of claims 14-17 and 31-34 is respectfully requested.

Claims 35-40, 42, and 43 have been rejected under 35 U.S.C. § 103(a) over the '072 patent in view of S. Wolf, *Silicon* Processing ("*Wolf*") for the reasons stated on pages 26-34 of the Office Action. Applicants respectfully traverse.

Claim 35 recites, *inter alia*, "forming a polysilicon layer upon said oxide layer." This polysilicon layer serves as an etch stop in various embodiments of the invention. *See e.g.* page 6, ll.

15-17. The '072 patent has no such teaching or suggestion of this feature of the invention.

Additionally, claims 35, 38, and 42 recite some form of planarization that is performed in the absence of masking of a conformal layer over at least one isolation trench. In contrast, this feature is clearly not taught or suggested in the '072 patent. Rather, as previously described the '072 patent discloses a more complicated method that involves masking of a conformal layer and other steps.

In addition, present claim 43 recites, *inter alia* and with language variations in each claim, "planarizing the *conformal layer* ... to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces" (emphasis added). In contrast, the method disclosed in the '072 patent relies then on the deposition of reverse-resist mask 368 over trench regions 356 (*see* the '072 patent, Fig. 3K, col. 4, *ll.* 51-52) to subsequently perform a wet or dry etch to partially remove oxide layer 364 and leave a remaining oxide layer 364 with ridges 373 (*see* the '072 patent, Fig. 3L, col. 4, *ll.* 52-54). It is this reduced oxide layer 372 with oxide ridges 373 that is subsequently treated by chemical-mechanical polishing until silicon nitride layer 344 is exposed (*see* the '072 patent, Fig. 3M, col. 4, *ll.* 54-57, 59-61). Accordingly, the method disclosed in the '072 patent does not *planarize the conformal oxide layer* 364 to produce the structure with an upper surface for each isolation trench shown in Fig. 3M therein. Instead, the '072 patent relies upon a more complicated method with more steps.

Additionally, present claim 42 recites the use of a single etch recipe to form a planar upper surface from the conformal layer. In contrast, the method disclosed in the '072 patent, as previously noted, uses a multi-step method with different etch recipes to form a planar upper surface.

Wolf cannot cure the foregoing deficiencies of the '072 Patent. Claims 36, 37, 29, and 40 depend from one of independent 35 and 38, respectively, and include the limitations recited therein.

Accordingly, for at least the reasons presented above with respect to claims 35 and 38, claims 36, 37, 29, and 40 are not obviated by the '072 patent in view of *Wolf*. Accordingly, the prompt removal of the rejection of claims 35-40, 42, and 43 is respectfully requested.

Claims 5 and 20 have been rejected under 35 U.S.C. § 103(a) over the '072 patent and the '108 patent and further in view of *Wolf* or *Poon*. Applicants respectfully traverse.

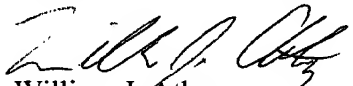
Claims 5 and 20 depend from independent claims 1 and 18, respectively, and include the limitations recited therein. Accordingly, for at least the reasons presented above with respect to claims 1 and 18, claims 5 and 20 are not obviated by the '072 patent and the '108 patent. *Wolf* and *Poon* cannot overcome the deficiencies of the '072 patent and the '108 patent with respect to claims 1 and 18. Accordingly, the prompt removal of the rejection of claims 5 and 20 is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 30th day of September 2003.

Respectfully submitted,



William J. Athay
Attorney for Applicants
Registration No. 44,515
Customer No. 022901

Telephone: (801) 533-9800
Fax: (801) 328-1707

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